Sole Inventor

Docket No. 20059/PIA31212

"EXPRESS MAIL" mailing label No.
EV 403728085 US
Date of Deposit: **December 30, 2003**

I hereby certify that this paper (or fee) is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 CFR §1.10 on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Jae Suk LEE**, a citizen of the Republic of Korea, residing at 891-10 Daechi-dong, Gangnam-gu, Seoul, Korea have invented new and useful **METHODS FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURES**, of which the following is a specification.

METHODS FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURES

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to semiconductor devices; and, more particularly, to methods for forming shallow trench isolation structures.

BACKGROUND

[0002] In semiconductor devices such as transistors, an isolation region is needed to prevent leakage current from occurring between devices. Shallow trench isolation (STI) structures have been widely used to form these isolation regions in semiconductor devices.

[0003] The STI structures are generally formed as follows. A pad dielectric pattern is formed on a silicon substrate. Shallow trenches are formed by etching the silicon substrate using the pad dielectric pattern as a mask. A dielectric layer is deposited to fill the trench. A planarization process is performed on the dielectric layer.

[0004] However, during such a procedure, the pad dielectric pattern may be easily damaged during the etching process of the silicon substrate. This damage causes a leakage problem in the devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figs. 1A to 1G are cross-sectional views illustrating example processes of manufacturing a shallow trench isolation structure in accordance with the teachings of the present disclosure.

[0006] Figs. 2A to 2G are cross-sectional views illustrating example processes of manufacturing a shallow trench isolation structure in accordance with the teachings of the present disclosure.

DETAILED DESCRIPTION

[0007] Fig. 1A shows a formation of a LP-TEOS (Low Pressure Tetra Ethyl Ortho Silicate) oxide layer 12 and a nitride layer 14 on a surface of a substrate 10 by using, for example, LPCVD (Low Pressure Chemical Vapor Deposition) in sequence. The LP-TEOS oxide layer 12 and the nitride layer 14 have thickness ranging about from 1000 to 5000 angstroms and from about 1000 to 10000 angstroms, respectively. Further, in the LPCVD process, the LP-TEOS oxide layer 12 or the nitride layer 14 is preferably formed at a temperature ranging from about 800 to 1200 °C and a pressure ranging from about 0 to 5 torr.

[0008] Next, a PR (Photo Resist) pattern 16 is formed on the nitride layer 14 to define trench regions thereon. The thickness of the PR pattern 16 preferably ranges from about 1000 to 10000 angstroms.

[0009] With reference to Fig. 1B, using the PR pattern 16 as a mask, the LP-TEOS oxide layer 12 and the nitride layer 14 are then etched to thereby form a LP-TEOS oxide pattern 12 and a nitride pattern 14. The etching

process may be performed by using, for example, an RIE (Reactive Ion Etching) method. The PR pattern 16 is then removed or stripped.

[0010] Subsequently, as shown in Fig. 1C, trenches are formed through the LP-TEOS oxide layer 12 and the nitride layer 14 and partially into the substrate 10. The substrate 10 is etched to a predetermined depth using the nitride pattern 14 as a mask. The etching process may be carried out by using an RIE method. An etched part of the substrate 10, the LP-TEOS oxide pattern 12, and the nitride pattern 14 form a hollow space, (i.e., a trench). The depth of the trench preferably ranges from about 2000 to 6000 angstroms. Further, the trench has sidewalls and a bottom.

[0011] Thereafter, an oxide layer 18 is formed on an entire surface of the device, (i.e., on the surface of the nitride pattern 14 and the surface of the sidewalls and the bottom of the trench) as shown in Fig. 1D. The oxide layer 18 may contain LP-TEOS oxide or thermal oxide and have a thickness ranging from about 100 to 1000 angstroms.

[0012] Referring to Fig. 1E, a metal or poly-silicon layer 20 is formed on the oxide layer 18 through the use of, for example, a sputtering process. Further, the metal or poly-silicon layer 20 may contain poly-silicon, laminated metal of Ti, TiN and W or laminated metal of Ta, TaN and W. The laminated metal of Ti, TiN and W is formed by sequentially laminating Ti, TiN and W layers. The preferred thicknesses of the Ti, TiN and W layers range from about 30 to 100 angstroms, from about 50 to 200 angstroms, and from about 50 to 200 angstroms, respectively. Further, the laminated metal of Ta, TaN and W is made by sequentially laminating Ta, TaN and W layers. The

preferred thicknesses of Ta, TaN and W layers are equivalent to those of Ti, TiN and W layers, respectively. When poly-silicon is used to form the metal or poly-silicon layer 20, the preferred thickness ranges from about 100 to 300 angstroms.

[0013] Referring to Fig. 1F, portion(s) of the metal or poly-silicon layer 20 are removed such that the oxide layer 18 on the bottom of the trench(es) are exposed, while leaving the metal or poly-silicon layer 20 on the sidewalls of the trench(es).

[0014] In a first example, each of the sidewalls of the metal or poly-silicon layer 20 may act as a floating metal or floating poly-silicon. That is, the sidewalls are separated from each other.

[0015] With reference to Fig. 1G, a dielectric material layer 22, (e.g., an oxide layer), is deposited to fully fill the trench(es) by using an HDP CVD (High Density Plasma Chemical Vapor Deposition) or an O_3-TEOS CVD (Ozone - Tetra Ethyl Ortho Silicate Chemical Vapor Deposition) method. Next, a planarization process, (e.g., a chemical mechanical planarization), may be performed. That is, the dielectric material layer 22 is polished until a surface of the nitride pattern 14 is exposed. Consequently, the first example STI structures are completed.

[0016] The sidewalls of the metal or poly-silicon layer 20 may trap electrons to thereby prevent the electrons from moving. That is, the sidewalls may accumulate charges to thereby reduce leakage between semiconductor devices.

[0017] In the following, a second example process will be described in detail with reference to Figs. 2A to 2G. In the second example, the processes of forming the LP-TEOS oxide layer 12 and the nitride layer 14 and forming the trench(es) are the same as those of the above-described with respect to the example of Figs. 1A-1C. Therefore, in the interest of avoiding undue repetition, only the processes following the formation process of the trench(es) will be described for the second example, and the processes associated with Figs. 2A-2C will not be repeated here. Instead, the interested reader is referred to the description of Figs. 1A-1C for a description of the processes illustrated in Figs. 2A-2C.

[0018] With reference to Fig. 2D, a first oxide layer 18 is formed on the entire surface of the device, (i.e., a surface of the nitride pattern 14 and a surface of the sidewalls and the bottom of the trench(es)). The first oxide layer 18 may contain LP-TEOS oxide or thermal oxide and have a thickness ranging from about 100 to 1000 angstroms.

[0019] Referring to Fig. 2E, a second oxide layer 20 is formed on the first oxide layer 18 and contains, for example, HDP CVD oxide or O_3-TEOS oxide. The second oxide layer 20 may have a thickness ranging from about 100 to 1000 angstroms.

[0020] Referring to Fig. 2F, a PSG (Phosphor Silicon Glass) layer 22 is formed on the second oxide layer 20 by using an HDP CVD or O_3-TEOS CVD method. Preferably, the PSG layer has a thickness ranging from about 100 to 100 angstroms.

[0021] Referring to Fig. 2G, a USG (Undoped Silicon Glass) layer 24 is deposited to fully fill the trench(es) by using an HDP CVD or O_3-TEOS CVD method. Next, a planarization process, (e.g., a chemical mechanical planarization), may be performed. That is, the USG layer 24 is polished until a surface of the nitride pattern 14 is exposed. Consequently, the second example STI structures are completed.

[0022] In the second example, the PSG layer 22 may act in the same manner as the sidewalls of the metal or poly-silicon layer 20 does in the first example. That is, the PSG layer 22 may accumulate charges to thereby reduce leakage between the semiconductor devices.

[0023] From the foregoing, persons of ordinary skill in the art will appreciate that the above disclosed methods form a shallow trench isolation structure having reduced leakage by inserting floating metal or floating poly-silicon into a shallow trench structure.

[0024] In a disclosed example, a trench is formed in a substrate and then an oxide layer is formed on sidewalls and a bottom of the trench. Thereafter, a metal or poly-silicon layer is formed on the oxide layer. Next, a portion of the metal or poly-silicon layer is etched such that the oxide layer on the bottom of the trench is exposed, while leaving the metal or poly-silicon layer on the sidewalls of the trench. Finally, a dielectric material layer is deposited to fully fill the trench.

[0025] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of

manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.